Jayawant Shikshan Prasarak Mandal's

JSPM Narhe Technical Campus

S.No.12/2/2 and 14/9 Narhe, **Tal**: Haveli, **Dist.**:Pune-411041
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Approved by AICTE New Delhi and DTE Maharashtra
Affiliated to Savitribai Phule Pune University

Prof.(Dr.)T. J.Sawant
B.E.(Elec.), PGDM,Ph.D
Founder - Secretary

Prof.(Dr.) R.K.Lad
B.E.(Civil),M.E.(Env.Engg.),Ph.D(Engg.)
DIRECTOR

Date: 29/10/2018

To

The Coordinator,

NAAC, Bengaluru

Subject: Proofs of new courses introduced during last five years

Reference: 1.2.1 Percentage of new courses introduced of the total number of courses across all programs offered during the last five years.

Dear Sir/Madam,

Year wise new courses introduced during last five years are mentioned in below table. Some sample syllabus structures and circulars are attached herewith this letter. The detailed list of courses is given on the link:

http://jspmntc.edu.in/Criteria-I/pdf/C1/1.2.1.pdf

J.S.P.M. Narhe Technical Campus Narhe Pune-41

Dr. R. K. Lad
Director
J.S.P.M. Narhe, Technical Campus
Narhe Pune-41

Director

Enclosures:

1. Sample University circular regarding syllabus change
2. Syllabus structure

सावित्रीबाई फुले पुणे विद्यापीठ

(पूर्वीचे पुणे विद्यापीठ)

दूरध्वनी क्रमांक :
०२०—२५६९१२३३
२५६०१२५८
२५६०१२५९

शैक्षणिक विभाग
गणेशखिंड, पुणे—४११ ००७
टेलिग्राफ : 'युनिपुणे'
फॅक्स : ०२०—२५६९१२३३
वेबसाइट : www.unipune.ac.in
इ—मेल : boards@pun.unipune.ac.in

संदर्भ क्र. :सी.बी./इंजि. / 296

दिनांक : 03/05/2017

परिपत्रक क्रमांक. 83 /२०१७

विषय :— अभियांत्रिकी विद्याशाखेंतर्गत एम.ई. २०१७ पॅटर्न पदव्युत्तर पदवी अभ्यासक्रमाचा सुधारित आराखडा व अभ्यासक्रम शैक्षणिक वर्ष २०१७—१८ पासून लागू करण्याबाबत.....

विद्यापीठ अधिकार मंडळाने घेतलेल्या निर्णयानुसार सर्व संबंधितांस या परिपत्रकाद्वारे कळविण्यात येते की, अभियांत्रिकी विद्याशाखेंतर्गत एम.ई. २०१७ पॅटर्न पदव्युत्तर पदवी अभ्यासक्रमांचा सुधारित आराखडा व अभ्यासक्रमास शैक्षणिक वर्ष २०१७—१८ पासून मान्यता देण्यात येत आहे.

सदर अभ्यासक्रम सावित्रीबाई फुले पुणे विद्यापीठाच्या www.unipune.ac.in या वेबसाईटवर Syllabi– Engineering या शीर्षकाखाली उपलब्ध आहे.

सावित्रीबाई फुले पुणे विद्यापीठाच्या सर्व संलग्न अभियांत्रिकी महाविद्यालयांचे मा. प्राचार्य यांना विनंती की, सदर परिपत्रकाचा आशय सर्व सबंधित प्राध्यापक व विद्यार्थ्यांच्या निदर्शनास आणून द्यावा.

उपकुलसचिव
(शैक्षणिक विभाग)

कृ. मा. प.

प्रत माहितीसाठी व पुढील योग्य त्या कार्यवाहीसाठी:—

१. मा. समन्वयक, अभियांत्रिकी विद्याशाखा
२. मा. संचालक, म.वि.वि.मं
३. मा. प्राचार्य, सर्व अभियांत्रिकी महाविद्यालये
४. मा. संचालक, सर्व मान्यताप्राप्त संस्था
५. मा. परीक्षा नियंत्रक, सा. फु. पुणे विद्यापीठ
६. मा. संचालक, स्पर्धा परीक्षा केंद्र
७. मा. उपकुलसचिव, परीक्षा (१,२)
८. मा. सिस्टीम ॲनालिस्ट डेटा प्रोग्रेसिंग युनिट
९. मा. उपकुलसचिव, नियोजन व विकास
१०. मा. उपकुलसचिव, (पात्रता विभाग)
११. मा. उपकुलसचिव (सभा दप्तर)
१२. मा. संचालक (आंतरराष्ट्रीय केंद्र)
१३. सहायक कुलसचिव, शैक्षणिक प्रवेश विभाग
१४. सहायक कुलसचिव (गोपनीय कक्ष)
१५. सहायक कुलसचिव (परीक्षा—एस.ॲण्ड टी. विभाग)
१६. सहायक कुलसचिव (परीक्षा समन्वय)
१७. वरिष्ठ कायदा अधिकारी
१८. जनसंपर्क अधिकारी
१९. कक्षाधिकारी (बहि:स्थ)
२०. प्रमुख, विद्यापीठ उपकेंद्र : अहमदनगर, नाशिक.

वि.प. ठराव क्र. ब ०५ पीए/०५/२०१६, दि. २९ नोव्हेंबर, २०१६

Third Engineering-E&TC (2015 Course)

(With effect from Academic Year 2017-18)

Semester I												
Course Code	**Course**	**Teaching Scheme Hours / Week**			**Semester Examination Scheme of Marks**						**Credits**	
		Theory	**Tutorials**	**Practicals**	**In-Sem**	**End-Sem**	**TW**	**PR**	**OR**	**Total**	**TH/TW**	**PR+OR**
304181	Digital Communication	4	--	--	30	70	--	--	--	100	4	--
304182	Digital Signal Processing	4	--	--	30	70	--	--	--	100	4	--
304183	Electromagnetics	3	1	--	30	70	--	--	--	100	4	--
304184	Microcontrollers	3	--	--	30	70	--	--	--	100	3	1
304185	Mechatronics	3	--	--	30	70	--	--	--	100	3	1
304191	Signal Processing and Communications Lab (DC/DSP)	--	--	4	--	--	50	50		100	--	2
304192	Microcontrollers and Mechatronics Lab	--	--	4	--	--	50	50		100		
304193	Electronics System Design	2	--	2	--	--	-	--	50	50	2	1
	Audit Course 3	--	--	--	--	--	--	--	--	--	----	
	Total	19	1	10	150	350	100	100	50	750		
										Total Credits	**25**	

Abbreviations:

TH: Theory **OR: Oral**
TW: Term Work **PR: Practical**

Note: Interested students of T.E (Electronics/E&TC) can opt any one of the audit course from the audit courses prescribed by BoS (Electronics/Computer/IT/Electrical/Instrumentation)

Third Engineering-E&TC (2015 Course)

(With effect from Academic Year 2017-18)

Semester II												
Course Code	**Course**	**Teaching Scheme Hours / Week**			**Semester Examination Scheme of Marks**						**Credit**	
		Theory	**Tutorials**	**Practicals**	**In-Sem**	**End-Sem**	**TW**	**PR**	**OR**	**Total**	**TH/TW**	**PR +OR**
304186	Power Electronics	4	--	--	30	70	--	--	--	100	4	--
304187	Information Theory, Coding and Communication Networks	4	--	--	30	70	--	--	--	100	4	--
304188	Business Management	3	--	--	30	70	--	--	--	100	3	--
306189	Advanced Processors	4	--	--	30	70	--	--	--	100	4	1
304190	System Programming and Operating Systems	3	--	--	30	70		--	--	100	3	1
304194	Power and ITCT Lab	--	--	4	--	--	50	50	--	100	--	2
304195	Advanced Processors and System Prograaming. Lab	--	--	4	--	--	50	50	--	100		
304196	Employability Skills and Mini Project	2	--	2	--	--	--	--	50	50	2	1
	Audit Course 4	--	--	--	--	--	--	--	--	--		
	Total	20	---	10	150	350	100	100	50	750		
										Total Credits	**25**	

Abbreviations:

TH: Theory **OR: Oral**
TW: Term Work **PR: Practical**

Note: Interested students of T.E (Electronics/E&TC) can opt any one of the audit course from the audit courses prescribed by BoS (Electronics/Computer/IT/Electrical/Instrumentation)

M.E. (Electronics and Telecommunications-
VLSI and Embedded Systems)

2017 Pattern
Syllabus Structure

First Year – Semester I

Sr.No.	Subject Code	Subject	Examination Scheme					Total	Credits
				Paper					
			L/P	ISA	ESA	TW	OR		
1	504201	Digital CMOS Design	4	50	50	-	-	100	4
2	504202	Reconfigurable Computing	4	50	50	-	-	100	4
3	504203	Embedded System Design	4	50	50	-	-	100	4
4	504204	Research Methodology	4	50	50	-	-	100	4
5	504205	Elective I	5	50	50	-	-	100	5
6	504206	Lab. Practice I	4	-	-	50	50	100	4
		Total	**25**	**250**	**250**	**50**	**50**	**600**	**25**

Elective I:

1. Micro Electromechanical Systems
2. Nano Technology
3. Processor Design
4. Wireless Sensor Networks
5. MOS Device Modeling and Characterization

First Year – Semester II

Sr.No.	Subject Code	Subject	Examination Scheme					Total	Credits
				Paper					
			L/P	ISA	ESA	TW	OR		
1	504207	Analog CMOS Design	4	50	50	-	-	100	4
2	504208	System on Chip	4	50	50	-	-	100	4
3	504209	Embedded Automotive Systems	4	50	50	-	-	100	4
4	504210	Elective II	5	50	50	-	-	100	5
5	504211	Lab. Practice II	4	--	---	50	50	100	4
6	504212	Seminar I	4	-	-	50	50	100	4
		Total	**25**	**200**	**200**	**100**	**100**	**600**	**25**

Elective II :

1. Embedded Product Design
2. High Speed ICs
3. Mixed Signal IC Design
4. Embedded Signal Processor Architectures
5. Real Time Operating Systems

Second Year – Semester I

Sr.No.	Subject Code	Subject	Examination Scheme					Total	Credits
				Paper					
			L/P	ISA	ESA	TW	OR		
1	604201	Testing and Verification ofVLSI Circuits	4	50	50	-	-	100	4
2	604202	ASIC Design	4	50	50	-	-	100	4
3	604203	Elective III	5	50	50	-	-	100	5
4	604204	Seminar II	4	--	----	50	50	100	4
5	604205	Project Stage I	8	--	---	50	50	100	8
		Total	**25**	**150**	**150**	**100**	**100**	**500**	**25**

Elective III:

Elective III Topics for 3 Credits

1 Value Education, Human Rights and Legislative Procedures
2 Environmental Studies
3 Renewable Energy Studies
4 Disaster Management
5 Foreign language
6 Knowledge Management
7 Economics for Engineers
8 Engineering Risk – Benefit Analysis

Elective III Topics for 2 Credits

1 Optimization Techniques
2 Fuzzy Mathematics
3 Design and Analysis of Algorithms
4 CUDA

Second Year – Semester II

Sr.No.	Subject Code	Subject	Examination Scheme					Total	Credits
				Paper					
			L/P	ISA	ESA	TW	OR		
1	604206	Seminar III	5	--	----	50	50	100	5
2	604207	Project Stage II	20	--	---	150	50	200	20
		Total	**25**		**--**	**200**	**100**	**300**	**25**

Note: Seminar I, II & III reports should be prepared in Latex.

Savitribai Phule Pune University, Pune
SE(E&TC/Electronics Engineering) 2015 Course

(With effect from Academic Year 2016-17)

Semester I

Course Code	Course	Teaching Scheme Hours / Week			Semester Examination Scheme of Marks						Credit	
		Theory	Tutorials	Practicals	In-Sem (On line)	End-Sem (Theory)	TW	PR	OR	Total	TH/TUT	PR+OR
204181	Signals & Systems	3	1	-	50	50	25	-	-	125	4	-
204182	Electronic Devices & Circuits	4	-	2	50	50	-	50	-	150	4	1
204183	Electrical Circuits and Machines	3	-	2	50	50	25	-	-	125	3	1
204184	Data Structures and Algorithms	4	-	2	50	50	-	-	50	150	4	1
204185	Digital Electronics	4	-	2	50	50	-	50	-	150	4	1
204186	Electronic Measuring Instruments & Tools	1	-	2	-	-	50	-	-	50	1	1
204192	**Audit Course 1**	--	--	--	--	--	--	--	--	--		
	Total	19	1	10	250	250	100	100	50	750	20	05
										Total Credits	**25**	

Abbreviations:

Th : Theory
TW: Term Work
OR: Oral
TUT : Tutorial
PR : Practical

Note: Interested students of S.E. (Electronics/E&TC) can opt any one of the audit course from the audit courses prescribed by BoS (Electronics/Computer/IT/Electrical/Instrumentation)

SE(E&TC/Electronics Engineering) 2015 Course

(With effect from Academic Year 2016-17)

Semester II

Course Code	Course	Teaching Scheme Hours / Week			Semester Examination Scheme of Marks						Credit	
		Theory	Tutorials	Practicals	In-Sem (on line)	End-Sem (Theory)	TW	PR	OR	Total	TH/TUT	PR+OR
207005	Engineering Mathematics III	4	1	-	50	50	25	-	-	125	5	-
204187	Integrated Circuits	4	-	2	50	50	25	50	-	175	4	1
204188	Control Systems	3	-	-	50	50	-	-	-	100	3	-
204189	Analog Communication	3	-	2	50	50	-	50	-	150	3	1
204190	Object Oriented Programming	3	-	4	50	50	-	-	50	150	3	2
204191	Employability Skill Development	2	-	2	-	-	50	-	-	50	2	1
204193	**Audit Course 2**	--	--	--	--	--	--	--	--	--		
	Total	19	1	10	250	250	100	100	50	750	20	05
									Total Credits		**25**	

Abbreviations:

TH: Theory
TW: Term Work
OR: Oral
TUT: Tutorial
PR: Practical

Note: Interested students of S.E (Electronics/E&TC) can opt any one of the audit course from the audit courses prescribed by BoS (Electronics/Computer/IT/Electrical/Instrumentation)

BE (E & TC) Structure
2012 Course w.e.f. June 2015
Semester-I

Subject Code	Subject	Teaching Scheme			Examination Scheme					Marks
		LECT	TUT	PR	In Semester Assessment Phase I	PR	OR	TW	End Semester Examination Phase II	Total
404181	VLSI Design & Technology	3			30				70	100
404182	Computer Networks	3			30				70	100
404183	Microwave Engineering	4			30				70	100
404184	Elective I	3			30				70	100
404185	Elective II	3			30				70	100
404186	Lab Practice I (CN & MWE)			4			50	50		100
404187	Lab Practice II (VLSI &Elective I)			4		50		50		100
404188	Project Phase I		2				50			50
	Total	**16**	2	8	150	50	100	100	350	750

Elective I

1. Digital Image Processing
2. Embedded Systems & RTOS
3. Software Defined Radio
4. Industrial Drives and Control

Elective II

1. Multi rate & Adaptive Signal Processing
2. Electronic Product Design
3. PLCs and Automation
4. Artificial Intelligence

Semester-II

Subject Code	Subject	Teaching Scheme			Examination Scheme					Marks
		LECT	TUT	PR	In Semester Assessment Phase I	PR	OR	TW	End Semester Examination Phase II	Total
404189	Mobile Communication	4			30				70	100
404190	Broadband Communication Systems	4			30				70	100
404191	Elective III	3			30				70	100
404192	Elective IV	3			30				70	100
404193	Lab Practice III(MC & BCS)			4			50	50		100
404194	Lab Practice IV(Elective III)			2		50		50		100
404195	Project Phase II		6			50		100		150
	Total	**14**	**6**	**6**	**120**	**100**	**50**	**200**	**280**	**750**

Elective III

1. Speech & Audio Signal Processing
2. RF Circuit Design
3. Audio Video Engineering
4. Soft Computing

Elective IV

1. Biomedical Signal Processing
2. Nano Electronics & MEMS
3. Detection & Estimation Theory
4. Wireless Networks
5. Open Elective*

***Any one subject from the list of Elective IV of computer/IT/Electrical/Instrumentation or Institute can offer elective IV based on any industry need with prior approval from BoS(Electronics). Repetition of subjects or topics is to be avoided.**

Dr. D. S. Bormane
Chairman, BOS(Electronics)

TE (E & TC) Structure

(2012 Course w.e.f. June 2014)

SEMESTER I

Subject Code	Subject	Teaching Scheme			Examination Scheme					Marks
		Lect	Tut	Pr	In Semester Assessment Phase I	Pr	Oral	TW	End Semester Examination Phase II	Total
304181	Digital Communication	4			30				70	100
304182	Digital Signal Processing	4			30				70	100
304183	Micro Controller and Applications	3			30				70	100
304184	Electromagnetics and Transmission Lines	3	1		30				70	100
304185	System Programming and Operating System	3			30				70	100
304186	Digital Communication and Signal Processing Lab			4		50		50		100
304187	System Programming and Microcontroller Applications Lab			4		50		50		100
304188	Employability Skills in Electronics Design	2		2			50			50
	Total	**19**	**1**	**10**	**150**	**100**	**50**	**100**	**350**	**750**

TE (E & TC) Structure

(2012 Course w.e.f. June 2014)

SEMESTER II

Subject Code	Subject	Teaching Scheme			Examination Scheme					Marks
		Lect	Tut	Pr	In Semester Assessment Phase I	Pr	Oral	TW	End Semester Examination Phase II	Total
304189	Information Theory and Coding Techniques	4			30				70	100
304190	Antenna and Wave Propagation	4			30				70	100
304191	Embedded Processors	4			30				70	100
304192	Industrial Management	3			30				70	100
304193	Power Electronics	3			30				70	100
304194	Communication Lab			4		50		50		100
304195	Power Electronics and Embedded Lab			4		50		50		100
304196	Mini project and Seminar			4			50			50
	Total	18		12	150	100	50	100	350	750

Course Structure for S.E. (Electronics/Electronics & Telecommunication Engineering)

2012 Course (w.e.f. June-2013)

SEMESTER-I										
Subject Code	**Subject**	**Teaching Scheme Hrs/Week**			**Examination Scheme**					**Marks**
		Lect	**Tut**	**Pr**	**Theory Online**	**Tw**	**Pr**	**Or**	**Theory Paper**	**Total**
204181	Signals & Systems	4	1	-	50	25	-	-	50	125
204182	Electronic Devices & Circuits	4	-	2	50	-	50	-	50	150
204183	Network Theory	3	1	-	50	25	-	-	50	125
204184	Data structures & Algorithms	4	-	2	50	-	-	50	50	150
204185	Digital Electronics	4	-	2	50	-	50	-	50	150
204186	Electronic Measuring Instruments & Tools	1	-	2	-	50	-	-	-	50
	Total	**20**	**2**	**8**	**250**	**100**	**100**	**50**	**250**	**750**
SEMESTER-II										
Subject Code	**Subject**	**Teaching Scheme Hrs/Week**			**Examination Scheme**					**Marks**
		Lect	**Tut**	**Pr**	**Theory Online**	**Tw**	**Pr**	**Or**	**Theory Paper**	**Total**
207005	Engineering Maths-III	4	1	-	50	25	-	-	50	125
204187	Integrated Circuits	3	-	2	50	-	50	-	50	150
204188	Control Systems	3	1	-	50	25	-	-	50	125
204189	Analog Communication	4	-	2	50	-	50	-	50	150
204190	Computer Organization	3	-	-	50	-	-	-	50	100
204191	Object Oriented Programming	2	-	2	-	25	-	50	-	75
204192	Soft Skills	1	-	2	-	25	-	-	-	25
	Total	20	2	8	250	100	100	50	250	750

Dr. D S Bormane
Chairman, BOS(Electronics)
University of Pune, Pune

University of Pune

COURSE STRUCTURE FOR M.E. (E & TC) (VLSI & Embedded Systems)
(w. e. f. June – 2013)

SEMESTER I

CODE	SUBJECT	TEACHING SCHEME	EXAMINATION SCHEME					CREDITS
		Lect./ Pr	Paper		TW	Oral/ Presentation	Total	
			In Semester Assessment	End Semester Assessment				
504201	Digital CMOS Design	4	50	50	-	-	100	4
504103	Embedded System Design	4	50	50	-	-	100	4
504203	Reconfigurable Computing	4	50	50	-	-	100	4
504104	Research Methodology	4	50	50	-	-	100	4
504205	Elective I	5	50	50	-	-	100	5
504206	Lab Practice I	4	-	-	50	50	100	4
Total		25	250	250	50	50	600	25

SEMESTER II

CODE	SUBJECT	TEACHING SCHEME	EXAMINATION SCHEME					CREDITS
		Lect./ Pr	Paper		TW	Oral/ Presentation	Total	
			In Semester Assessment	End Semester Assessment				
504207	Analog CMOS Design	4	50	50	-	-	100	4
504208	System on Chip	4	50	50	-	-	100	4
504209	Embedded Signal Processors	4	50	50	-	-	100	4
504210	Elective II	5	50	50	-	-	100	5
504211	Lab Practice II	4	-	-	50	50	100	4
504212	Seminar I	4	-	-	50	50	100	4
Total		25	200	200	100	100	600	25

SEMESTER III

CODE	SUBJECT	TEACHING SCHEME	EXAMINATION SCHEME					CREDITS
		Lect./ Pr	Paper		TW	Oral/ Presentation	Total	
			In Semester Assessment	End Semester Assessment				
604201	Fault Tolerant Systems	4	50	50	-	-	100	4
604202	ASIC Design	4	50	50	-	-	100	4
604103	Elective III	5	50	50	-	-	100	5
604204	Seminar II	4	-	-	50	50	100	4
604205	Project Stage I	08	-	-	50	50	100	8
Total		25	150	150	100	100	500	25

SEMESTER IV

CODE	SUBJECT	TEACHING SCHEME	EXAMINATION SCHEME				CREDITS
		Lect./ Pr	Paper	TW	Oral/ Presentation	Total	
604206	Seminar III	5	-	50	50	100	5
604207	Project Work Stage II	20	-	150	50	200	20
Total		25	-	200	100	300	25

Elective I	1. Mathematics for VLSI and Embedded Systems 2. Neural Networks In Embedded Applications 3. Processor Design 4. Wireless Sensor Network 5. *LATEX
Elective II	1. Embedded Product Design 2. VLSI Interconnections 3. Mixed Signal Circuit Design 4. Software Defined Radio 5. *Software Tools
Elective- III	1.Value Education, Human Rights and Legislative Procedures 2. Environmental Studies 3. Energy Studies 4. Disaster Management 5. Knowledge Management 6. Foreign Language 7. Economics for Engineers 8. Engineering Risk – Benefit Analysis 9. Technology Play 10. Optimization Techniques 11. Fuzzy Mathematics 12. Design and Analysis of Algorithms 13. CUDA

Note: Syllabus for Elective III is common for all discipline.